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Bulk and Interface effects on voltage linearity of ZrO$_2$–SiO$_2$ multilayered metal-insulator-metal capacitors for analog mixed-signal applications

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Quadratic voltage coefficient of capacitance (VCC) for ZrO$_2$–SiO$_2$ multilayered dielectric metal-insulator-metal capacitors depends strongly on the stacking sequence of the layered dielectrics. The quadratic VCC of an optimized SiO$_2$/ZrO$_2$/SiO$_2$ stack and ZrO$_2$/SiO$_2$/ZrO$_2$ stack were +42 and −1094 ppm/V$^2$, respectively, despite the same total SiO$_2$ and ZrO$_2$ dielectric thickness in the stack. The observed difference in quadratic VCC depending on dielectric stacking sequence is explained by taking into account both the interface and bulk dielectric responses to the applied voltage. © 2009 American Institute of Physics. [DOI: 10.1063/1.3182856]

The metal-insulator-metal (MIM) capacitor is one of the main components of analog/mixed-signal integrated circuits and radio frequency devices.$^{1,2}$ The key figures of merit used to characterize MIM capacitors are capacitance density ($C_{\text{density}}$) and capacitance voltage nonlinearity.$^3$ Higher $C_{\text{density}}$ is required for capacitor area scaling, which results in increased circuit density and reduced system cost. Reduced capacitance nonlinearity is a benchmark to improve the accuracy of the passive components, since shifts in capacitance can lead to distortions in analog signals or can be upconverted to higher frequencies in mixers and nonlinear circuit applications.$^4$ The voltage nonlinearity of capacitance is characterized by the quadratic equation in voltage

$$\frac{\Delta C}{C_0} = \frac{C(V) - C_0}{C_0} = \alpha V^2 + \beta V,$$

where $C_0$ is the capacitance at zero-bias and $\alpha$ and $\beta$ are the quadratic and linear coefficients of the capacitor, respectively.$^4$ The quadratic voltage nonlinearity is inversely proportional to the dielectric thickness (1/$t_{\text{ox}}$)$^2$; therefore, $\alpha$ and $C_{\text{density}}$ are in a trade-off relationship, making the simultaneous achievement of large $C_{\text{density}}$ and linearity difficult. Shown in Fig. 1 is published data for voltage coefficient of capacitance (VCC) versus $C_{\text{density}}$ plotted along with results of the present work. Many high-$k$ dielectrics, such as HfO$_2$,$^1$ Ta$_2$O$_5$,$^6$ and Al$_2$O$_3$,$^7$ have been investigated as an insulator in MIM capacitors, however, there is no known single-layer high-$k$ dielectric MIM capacitor that meets the International Technology Roadmap for Semiconductors (ITRS) guidelines for 2012 ($C_{\text{density}} > 5 \, \text{fF}/\mu\text{m}^2$, $\alpha < 100 \, \text{ppm/V}^2$, and leakage current $< 10^{-8} \, \text{A/cm}^2$).$^3$ Numerous MIM capacitors with various bilayer, sandwiched, and laminated dielectrics have also been investigated.$^6$–$^{10}$ Among these multilayered dielectric stack MIM capacitors, only the HfO$_2$/SiO$_2$ bilayer dielectric seems to meet the ITRS guidelines (shaded area in Fig. 1).$^{10}$

Despite numerous efforts to improve the voltage linearity of MIM capacitors, the basic mechanism controlling the $\alpha$ of the MIM capacitor is not yet well understood. Several models have been proposed to explain its voltage linearity, such as the occurrence of free carrier space charge relaxation,$^{11}$ nonlinearities of the metal-oxygen bond polarizability,$^{12}$ or electrode coupling and “hopping” conduction between vacancy sites.$^{13}$ These models explain voltage linearity either by a dielectric bulk effect or dielectric/electrode interface effect.

In our study, voltage linearity of MIM capacitors with asymmetric bilayered and symmetric trilayered ZrO$_2$–SiO$_2$ dielectric stacks deposited in various sequences were investigated to study the mechanism of capacitance variation, taking into account both the dielectric bulk and dielectric/electrode interface characteristics. By combining a high dielectric constant (∼39) ZrO$_2$ having positive $\alpha$ with high band gap SiO$_2$, having negative $\alpha$, along with interface engineering, we were able to fabricate MIM capacitors with high $C_{\text{density}}$ and low $\alpha$ as well as low leakage current.

MIM capacitors were fabricated by using TiN as both top and bottom electrodes. Dielectric film thickness was measured by ellipsometer. Capacitors with different areas were defined by photolithography and plasma etching. The typical capacitor area was 0.01 mm$^2$ (100×100 $\mu$m$^2$).

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Capacitance-voltage (C-V) measurements were performed on a precision LCR meter (Hewlett-Packard, 4284A) at 100 kHz with a (25 mV) ac sweeping signal. Current-voltage (I-V) characteristics were measured using a semiconductor parameter analyzer (Hewlett-Packard, 4156B). For all C-V and I-V measurements, the potentials were referred to the bottom electrode, creating an electron injection from the bottom electron with positive bias. Capacitance has been normalized to the capacitance measured at 0 V dc bias across the capacitor.

Figure 2 shows (a) the normalized capacitance characteristics for a MIM capacitor with ZrO$_2$/SiO$_2$ bilayer stack and (b) the I-V characteristics of such a structure. The inset shows VCC $\alpha$ and $\beta$ and capacitance density ($C_{\text{density}}$) as a function of the dielectric stack sequence.

![Figure 2](image_url)

**FIG. 2.** (a) Normalized capacitance characteristics for a MIM capacitor with ZrO$_2$/SiO$_2$ bilayer stack and (b) I-V characteristics of such a structure. The inset shows VCC $\alpha$ and $\beta$ and capacitance density ($C_{\text{density}}$) as a function of the dielectric stack sequence.

Figure 3 shows the normalized capacitance of MIM capacitors with SiO$_2$/ZrO$_2$/SiO$_2$ and ZrO$_2$/SiO$_2$/ZrO$_2$ stacks. Both stacks, denoted as S1 and S2, respectively, have similar capacitance density, as the inset shows, but significantly different quadratic VCC values depending on the dielectric deposition sequence.

![Figure 3](image_url)

**FIG. 3.** Normalized capacitance of MIM capacitors with SiO$_2$/ZrO$_2$/SiO$_2$ and ZrO$_2$/SiO$_2$/ZrO$_2$ stacks. Both stacks, denoted as S1 and S2, respectively, have similar capacitance density, as the inset shows, but significantly different quadratic VCC values depending on the dielectric deposition sequence.

role to achieve low $\alpha$ and high $C_{\text{density}}$ in a MIM capacitor.

Figure 3 shows the normalized capacitance of MIM capacitors with symmetric sandwiched dielectric stacks, but with different stacking order to see the effect of dielectric and electrode interface. The $C_{\text{density}}$ for the two different dielectric stacks is nearly the same, as shown in Fig. 3 (inset). The SiO$_2$/ZrO$_2$/SiO$_2$ and ZrO$_2$/SiO$_2$/ZrO$_2$ structures are denoted by S1 and S2, respectively. The total thicknesses of the ZrO$_2$ film and SiO$_2$ film in the symmetric sandwiched dielectric stacks are the same, as confirmed by high resolution transmission electron microscopy images (not shown). The $C_{\text{density}}$ of both S1 and S2 are close to 7.2 fF/um$^2$, with an equivalent oxide thickness (C) of around 4.8 nm. In contrast, S1 and S2 have very different $\alpha$ values despite their similar EOTs. The extracted $\alpha$ of S1 and S2 are $+42$ and $-1094$ ppm/V$^2$, respectively. If $\alpha$ is solely dictated by bulk dielectric properties,$^{11,12}$ there should not be a significant difference in the $\alpha$ of S1 and S2, which have the same total ZrO$_2$ and SiO$_2$ thicknesses, but with different stacking sequence. The SiO$_2$ layer is in contact with the TiN top and bottom electrode in S1, while the ZrO$_2$ layer is in contact with the TiN electrodes in S2. Alternatively, if $\alpha$ is determined solely by the dielectric/electrode interface effect, such as electrode polarization effect,$^{13}$ it is difficult to explain the negative $\alpha$ of S2. Our experimental data suggests that both dielectric bulk and dielectric/electrode interfaces are contributing to the $\alpha$ of the sandwiched structure. When a thin dielectric layer is in contact with electrodes, an electrode polarization exponentially increases the capacitance with applied voltage$^{13}$ (dielectric/electrode interface effect layer). When SiO$_2$ is in contact with the electrode as in S1, the negative $\alpha$ of SiO$_2$ is negated by the dielectric/electrode interface effect. But when SiO$_2$ is in the middle of a multilayer dielectric, the negative $\alpha$ characteristic of SiO$_2$ is maintained. Consequently, although S1 and S2 have the same SiO$_2$ thickness, the impact of SiO$_2$ in S2 is greater than in S1 and the $\alpha$ of S2 remains negative.

The impact of the dielectric/electrode interface effect on VCC characteristics for ZrO$_2$–SiO$_2$ multilayered MIM capacitors can be examined by using MIM capacitors with a single layer of SiO$_2$ having different thicknesses. Assuming that the dielectric/electrode interfacial layer is thinner than...
the SiO$_2$ dielectric thickness, the interface contribution to VCC will be greater as SiO$_2$ gets thinner. Figure 4 shows the normalized capacitance characteristics for single-layer SiO$_2$ MIM capacitors and the inset shows the corresponding leakage current as a function of applied electric field. To apply the same electric field to the MIM capacitors, the capacitance and leakage currents are measured with a voltage sweep from $-0.8$ to $0.8$ V, and from $-1.2$ to $1.2$ V, respectively. This contradicts the thickness dependency of $\alpha$, which predicts $\alpha$ being inversely proportional to the square of dielectric thickness, $\alpha \sim 1/t_{\text{SiO}_2}^2$. Since the thickness dependency of $\alpha$ takes into account only the bulk effect of the dielectric, the model fails to predict $\alpha$ of very thin dielectric layers in MIM capacitors where the interface effect is no longer negligible.

The voltage linearity of the high-$k$ MIM capacitors with ZrO$_2$–SiO$_2$ layered dielectrics was investigated as a function of stacking sequence. VCC of MIM capacitor was more positive when SiO$_2$ was in contact with electrodes than that of ZrO$_2$ being in contact with electrodes with same total SiO$_2$ and ZrO$_2$ thicknesses. This supports the concept that both electrode-dielectric interface and bulk dielectric effect play an important role in the voltage linearity of MIM capacitors. Effect of interface on VCC was confirmed with single-layer SiO$_2$ MIM capacitors, where lower absolute VCC was obtained in thinner SiO$_2$ in contrast to a model which only took into account bulk contribution to VCC. In addition, it has been shown that a MIM capacitor engineered with a symmetric layered dielectric stack of SiO$_2$–ZrO$_2$–SiO$_2$ can meet the ITRS guidelines for 2012.

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