Improvement of metal gate/high-\(k\) dielectric CMOSFETs characteristics by atomic layer etching of high-\(k\) gate dielectric

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1. Introduction

As the critical dimension (CD) of metal–oxide–semiconductor field effect transistor (MOSFET) is scaled down to tens of nanometer, the physical thickness of \(\text{SiO}_2\) is intrinsically limited. Therefore, high-\(k\) dielectrics having higher physical thickness with the same equivalent oxide thickness (EOT) are investigated as an alternative to \(\text{SiO}_2\). Among the numerous high-\(k\) dielectrics, hafnium oxide (\(\text{HfO}_2\)) has been presently integrated as the gate dielectric because it is stable and has a high dielectric constant (25), high thermal stability, and low interface states on the Si substrate[1].

For the high-\(k\) dielectric patterning, wet etching (WE) is used due to the thin thickness of the gate dielectric, the requirements of extremely high etch selectivity and low damage to the substrate. However, as the CD is scaled down to 32 nm and below, plasma etching such as reactive ion etching (RIE) gradually becomes more important because it is difficult for WE to etch anisotropically and remove compounds such as MeSiO\(_x\) formed at the interface between MeO\(_x\) and Si substrate. Even for plasma etching, it is important to etch with high etch selectivity over the substrate because the high-\(k\) dielectric must be etched from the source and drain regions without the silicon substrate recess. A previous study on \(\text{HfO}_2\) etching showed that a high etch selectivity to the silicon substrate can be achieved using Ar/C\(_4\)F\(_8\) gas compared to Ar/CF\(_4\) gas in an inductively coupled plasma (ICP) [2]. High etch selectivity greater than 10 over the silicon could be also achieved using BCl\(_3\)/Cl\(_2\) gas in an ICP [3]. However, plasma etching can introduce plasma induced damages (PIDs) and was found to degrade the electrical characteristics and reliability including the positive bias temperature instability (PBTI) and negative bias temperature instability (NBTI) in metal gate/high-\(k\) dielectric CMOSFETs [4–7].

There are two types of plasma induced damages (PIDs), which consist of plasma induced charging damage (PICD) and plasma induced edge damage (PIED) [8]. The former is originated from Fowler–Nordheim (FN) tunneling current through the gate oxide and the latter is caused by the direct \(\text{HfO}_2\) plasma interaction and ion bombardment at the edge of gate oxide. Especially, as the gate oxide thickness is decreased to nanoscale, due to the increase of direct tunneling, PIED becomes more important in PID.
Previously, to solve the PIED, gate re-oxidation and plasma O$_2$ treatment of gate oxide, etc. have been investigated [9–12]. Gate re-oxidation has been successfully introduced to poly-Si/SiO$_2$ [9] but, due to the increase of equivalent oxide thickness (EOT) and a change in the effective work function, it cannot be easily applied to poly-Si/TiN/HfO$_2$/Si [10]. Plasma O$_2$ treatment was also demonstrated to encapsulate and passivate the gate edge leakage path for high-k dielectric structures, but the process reliability and uniformity is still in question [11,12].

Atomic layer etching (ALE) has been previously investigated to etch the material with a precise etch rate without introducing physical and chemical damage to the substrate [13–15]. ALE is a cyclic process similar to atomic layer deposition (ALD), and it is consisted of four steps: (1) adsorption of reactive gas, (2) evacuation of un-reacted reactive gas, (3) desorption of chemisorbed compound by energetic particle beam bombardment, and (4) evacuation. However, after the one cycle, one atomic layer is etched for ALE instead of the deposition of one atomic layer. The details of the ALE can be found elsewhere [16]. Previous results on the ALE of HfO$_2$ showed the constant etch depth of an atomic layer scale per cycle without changing the chemical composition of the etched HfO$_2$ surface [17].

In this article, to study the effect of ALE for high-k dielectric on the device properties systematically, ALE has been applied to the high-k dielectric in a metal gate/high-k dielectric CMOSFET, and its electrical characteristics were compared with those obtained after the etching of HfO$_2$ by WE and RIE.

2. Experimental

Metal gate/high-k dielectric CMOSFET devices with a gate width ($W$) of 10 µm and length ($L$) of 1 µm were fabricated using a standard complementary MOS process. The gate structure was consisted of chemical vapor deposition (CVD) deposited 1000 Å poly-Si, atomic layer deposition (ALD) deposited 100 Å TiN, 30 Å HfO$_2$, and 10 Å interfacial SiO$_2$ over Si substrate. Using a hard mask (HM), after metal gate etching by a conventional reactive ion etching (RIE), HfO$_2$ was etched with wet etching (WE) (the standard HM), after metal gate etching by a conventional reactive ion etching after the activation of HfO$_2$ with an Ar physical bombardment, using a HF based solution, or RIE (a BCl$_3$/Cl$_2$ inductively couple plasma with —60 V of dc bias voltage), or ALE (a HF based solution) etching. These steps are a cyclic process similar to atomic layer deposition (ALD), and it is consisted of four steps: (1) adsorption of reactive gas, (2) evacuation of un-reacted reactive gas, (3) desorption of chemisorbed compound by energetic particle beam bombardment, and (4) evacuation. However, after the one cycle, one atomic layer is etched for ALE instead of the deposition of one atomic layer. The details of the ALE can be found elsewhere [16]. Previous results on the ALE of HfO$_2$ showed the constant etch depth of an atomic layer scale per cycle without changing the chemical composition of the etched HfO$_2$ surface [17].

3. Results and discussion

Fig. 1 shows the characteristics of drain current ($I_D$)–gate voltage ($V_G$) for NMOSFET (the $W/L$ of the device = 10/1 µm) after WE, RIE, and ALE. On-state current ($I_{on}$) at $V_D = V_{th} + 0.85$ V and $V_D = 1.2$ V for all devices was similar but, off-state current ($I_{off}$) at $V_C = 0$ V and $V_D = 1.2$ V for ALE was much lower than that for RIE while a slightly lower than that for WE, which was mainly attributed to the gate leakage current ($I_{leak}$) generated by PIED.

In fact, the $I_{leak}$ can be also affected by the etched gate edge profile of the high-k dielectric. The protruded high-k dielectric tend to decrease the $I_{leak}$ while the laterally recessed one tend to increase $I_{leak}$ due to the formation of the leakage path in the heterogeneous interface between the high-k dielectric and the capping nitride layer [18]. The origin of the change of $I_{leak}$ can be estimated by measuring gate-induced drain current ($I_{GILD}$), which is affected by the gate edge profile such as bird’s beak. As shown in Fig. 1, the measured $I_{GILD}$ values for WE, RIE, and ALE are similar to one another, respectively, suggesting that there is no significant change in the physical gate profile for WE, RIE, and ALE in a long channel device ($L = 1$ µm) investigated in this study. Therefore, the lowest $I_{leak}$ for ALE is believed to be caused by the decreased PIED instead of the gate profile during the high-k dielectric patterning.

Among the MOS parameters, gate leakage current ($I_{leak}$) is the most sensitive to PIED because it changes the state of the gate oxide edge, which results in increasing the perimeter component rather than area one due to the formation of the additional $I_{leak}$ path at the edge of gate oxide near the source and drain (S/D) regions. Therefore, to classify $I_{leak}$ into the area and perimeter component, MOSCAP with shallow trench isolation (STI) and MOSFET with source/drain (S/D) structure were used. In the case of MOSCAP, due to the smaller gate oxide edge area compared to gate oxide area, $I_{leak}$ of MOSCAP tends to be more sensitive to the area than perimeter component of $I_{leak}$. Therefore, the gate current density ($J_{G}$) of MOSCAPs with an area of $2 \times 10^{-4}$ cm$^2$ was measured as a function of $V_C$ after WE, RIE, and ALE as shown in Fig. 2a for PMOSCAP and NMOSCAP. No differences in $J_G$ were found among them indicating that the area component of $I_{leak}$ was maintained. However, Fig. 2b shows the gate current density–gate voltage ($J_G$–$V_G$) measured for NMOSFET and PMOSFET (not shown here) with a $W/L = 10/1$ µm after WE, RIE, and ALE. The $J_G$–$V_G$ could be divided into two distinctive regions. For the low $V_C$ region, ALE exhibited a much lower $J_G$ than RIE while showing a slightly lower $I_{leak}$ than WE. In contrast, at the high $V_C$ region, the differences in $J_G$ among them were decreased. It is known that, at the low $V_C$ region, the gate tunneling current flows primarily to the edge of gate oxide near the S/D regions while the current mainly flows through the gate oxide at the high $V_C$ region. Higher gate leakage current for WE, RIE compared to ALE at the low $V_C$ region could be originated from the perimeter component of $I_{leak}$ by the PIED rather than the area one, which resulted in increasing $I_{leak}$ as shown in Fig. 1.

To investigate the effect of PIED on gate oxide edge further, by using perimeter gate structure having the different length of gate dense line to increase the sidewall area of gate, the $J_G$ of NMOSFET was measured at the low $V_C$ region ($V_C = 0.5$ V), which is sensitive
to the perimeter component of $I_G$ by the PIED, after the etching by WE, RIE and ALE. As shown in the figure, the $I_G$ was significantly increased for the denser perimeter structured gates after RIE while showing no significant change for the different length of gate dense line after ALE. Therefore, after the ALE of the high-$k$ dielectric, the significant decrease of the PIED could be obtained.

In addition, to estimate the origin of the increased perimeter component of $I_G$ by PIED, the surface composition of HfO$_2$ surface was measured by X-ray photoelectron spectroscopy (XPS). By using ALE compared to RIE, the stoichiometry of HfO$_2$ surface is maintained during the HfO$_2$ patterning. Fig. 4 shows the atomic percentages of Hf and O on the HfO$_2$ surface measured by XPS during the each ALE cycle. As comparison, the atomic percentage ratios of Hf/O on the HfO$_2$ surface before the etching (as-is) and after RIE were also included. As shown in the figure, during the ALE, the atomic percentages of Hf and O were remaining similar during the ALE cycles because a monolayer was etched from the HfO$_2$ surface without the preferential removal of the component of HfO$_2$ such as Hf, or O per each cycle. Therefore, the atomic percentage ratio of Hf/O on the HfO$_2$ surface during ALE was also similar to that of as-is. However, in the case of RIE, the atomic percentage ratio of Hf/O was increased because it is preferentially etched more volatile component of HfO$_2$ such as BCl$_x$O$_y$ due to the higher vapor pressure of BCl$_x$O$_y$ formed as theetch products during the RIE. The change of surface composition during RIE will degrade the characteristics of HfO$_2$ by forming traps at the edge of the gate oxide near the S/D regions, which can be the additional gate leakage current path, therefore, the CMOSFETs etched by RIE showed noticeable PIED as observed in Figs. 1–3. However, by ALE, due to the no significant change of surface composition at the edge of gate oxide in addition to the exact silicon etch depth control, no significant PIED was observed.

4. Conclusions

In this study, ALE has been applied to the HfO$_2$ patterning after the TiN etching by RIE and its electrical characteristics of the CMOSFET were compared with those etched by WE or RIE. The CMOSFET etched by the ALE showed the improvement of $I_{off}$, which was mainly attributed to the decreased perimeter component of $I_G$ particularly, at the low field region due to PIED. These results were related to the low edge damage of gate oxide during the ALE by maintaining the surface composition at the edge of gate oxide in addition to the exact silicon etch depth control. It is believed that ALE is more beneficial to the high-$k$ dielectric patterning of next generation CMOSFET, which can be applicable to low standby power (LSTP) devices.

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